Abstract No: SC-26 **Smart Computing**

Developing a concept to convert LD/STL to VHDL

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Abstract

A Programmable Logic Controller (PLC) is a microprocessor based solid state device which is a very significant control component unit in industrial automation systems. Ladder diagram (LD) is a form of graphical language type PLC programming. LDs and Statement Lists (STL) are used to program PLCs. Both of these programming methods represent the schematics of electrical relay circuit diagram. Since LD programs are executed in a sequential and cyclic way, the operational efficiency and performance of PLC will be limited by the length of the ladder diagram and the operational speed of the microprocessor. Field Programmable Gate Array (FPGA) is a new technology used in industrial process control systems. VHDL (VHSIC-HDL-Very High Speed Integrated Circuit - Hardware Description Language) programming is used to program FPGA devices. Because of its parallel execution system and reconfigurable hardware structure, FPGA has excellent performance. Therefore, flexible and high speed systems can be implemented using FPGA. The main aspect of this research was to develop a concept to convert LD/STL to VHDL. By using Siemens - STEP 7 Micro/WIN - version 4.0.81 and Xilinx® – ISE Design Suite version 14.6 software, this concept was developed to convert Bit Logic LDs into VHDL. After identifying the Boolean logic of the STL code, inputs and outputs are declared in the entity part and PLC to FPGA conversion logic is defined in the architecture part of the VHDL code. To overcome the performance limitations of microprocessor based PLCs, FPGA based PLC implementation is suggested as a better approach.

Keywords: FPGA, LD, PLC, STL, VHDL

Introduction

Before the introduction of PLCs, mechanical relays were used to implement control systems. Ladder logic was used to document the design and construction of relay networks. With the invention of PLCs, ladder diagrams which is a form of graphical language type PLC programming, was introduced. Programming languages which are used to implement automation systems are standardized in IEC 61131-3 norm (Karl-Heinz et al., 1995).

Ladder Diagram programmes are executed in a sequential and cyclic way. Therefore, performance of PLC is limited. Operational efficiency and performance of PLC will be limited by the length of the ladder diagram and the operational speed of the microprocessor. In this research project FPGA based PLC implementation is suggested to overcome these drawbacks of PLCs. Some advantages of using FPGA to implement PLCs are parallel execution, reconfigurable hardware structure, high speed, increased flexibility, increased reliability and faster scanning time (Hauck & DeHon, 2008). IEEE 1076 is standardized for VHDL norm (IEEE Computer Society, 2008). A number of researches of this field have been conducted. In 1999 Ikeshita et al., developed a very rough manner to convert the LD into a program description of a very high speed integrated circuit VHDL (1999).